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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,084	FOGAL ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-19 and 24-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-19 and 24-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *110703* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6-19, and 24-32 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 8, 11, 13, 15, 17, and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana et al. (U.S. Patent 6,094,065) in view of (JP 6-232537).

In re claims 1, 8, 11, 13, 15, 17, and 24-32, **Tavana** discloses a method used to form a semiconductor device comprising: forming a semiconductor wafer section comprising first, second, and third pads thereon which are electrically separate from each other (**FIGS. 1-8** and related text); forming a first circuit portion **(FIG. 8: 12)**; forming a second circuit portion **(FIG. 8: 36)** and electrically isolated from the first circuit portion; forming a third circuit portion **(FIG. 8: 14)** and electrically isolated from the first and second circuit portions; and selectively electrically connecting together either the first and second circuit portions or the second and third circuit portions, wherein the semiconductor wafer section is enabled to function with a first operation mode if the first

and second pads are electrically connected together, and is enabled to function with a second operational mode different from the first operational mode if the second and third pads are electrically connected together (col. 7, lines 8-15 and **FIGS. 2-8**).

Tavana does not explicitly disclose wherein the first circuit portion electrically coupled with a first pad, the second circuit portion electrically coupled with the second pad, and the third circuit portion electrically coupled with the third pad and selectively electrically connecting together either the first and second pads or the second and third pads to electrically connect either the first and second circuit portions or the second and third circuit portions.

(JP 6-232537) discloses forming a first circuit portion (**FIGS. 3a-c: 11** (located on the left side in the drawing)) electrically coupled with a first pad (**FIGS. 3a-c: 12** (located on the left side in the drawing), a second circuit portion (**FIGS. 3a-c: 11** (located on the right side in the drawing)) electrically coupled with the second pad (**FIGS. 3a-c: 12** (located on the right side in the drawing)) and electrically connecting together the first and second pads to electrically connect the first and second circuit portions (**FIGS. 3b-c: 13**) (JP 6-232537 translation, pages 1-2). It would have been obvious to one of ordinary skill in the art to combine the teaching of Tavana and (JP 6-232537) to enable the process of selectively electrically connecting together the first and second pads to electrically connect the first and second circuit portions of Tavana to be performed and furthermore the short circuit of the electrode for closed circuit formation can be ensured (JP 6-232537 translation, page 1, paragraph [0008]).

In re claim 2, **Tavana** discloses attaching a single ball bond **(FIG. 8: 38)** to two of the pads during selective electrically connection (col. 7, lines 8-15).

2. Claims 3-4, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana et al. (U.S. Patent 6,094,065) in view of (JP 6-232537) as applied to claims 1, 2, 8, 11, 13, 15, 17, and 24-32 above, and further in view of Johnston (U.S. Patent 5,898,217).

In re claims 3-4 and 14, **Johnston** discloses attaching a wire bond **(FIG. 2, 128a)** to two of the pads **(FIG. 2, 121, 132)** during the selectively electrically connection comprising screen printing a conductive epoxy **(FIG. 2, 113)** to two of the pads (col. 2, line 53 to col. 3, line 19). It would have been obvious to one of ordinary skill in the art to combine the teaching of Tavana and Johnston to enable the process of attaching a wire bond and screen printing a conductive epoxy to the first and second bond pad portions of Tavana to be performed and furthermore to obtain an improved interconnect structure of a substrate of the packaged semiconductor device (col. 2, lines 21-31).

3. Claims 6, 7, 9, 10, 12, 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tavana et al. (U.S. Patent 6,094,065) in view of (JP 6-232537) as applied to claims 1, 2, 8, 11, 13, 15, 17, and 24-32 above, and further in view of the applicant's admitted prior art (AAPA) of this application

In re claim 6, **AAPA** discloses providing a transistor during providing the first circuit portion and providing one of a fuse and antifuse array during providing of the second circuit portion and selectively electrically connecting the first pad with the second pad thereby electrically coupling one of the fuse and antifuse array to the transistor

during selective electrical connection of the first and second pads (Background of the Invention on pages 2-3, paragraph [0005] and **FIG. 1** of this application). It would have been obvious to one of ordinary skill in the art to combine the teaching of Tavana and AAPA to electrically couple the fuse and antifuse array to the transistor during electrical connection of the first and second bond pad portions.

In re claims 7 and 12, **AAPA** discloses providing a lead frame and subsequent to selectively electrically connecting either the first and second pads or the second and third pads, attaching the wafer section to the lead frame (page 4, paragraph [0010]).

In re claims 9 and 10, **AAPA** discloses electrically coupling the second pad portion to the voltage source through a probe tip during the electrical coupling of the second pad portion with the voltage source; providing a CGND node during providing of second pad portion; electrically coupling the CGND node to the transistor during electrical coupling of the first pad portion with the second pad portion; and tying the CGND node to ground through the transistor during an operational mode of the semiconductor device subsequent to programming the array (pages 2-3, paragraph [0005] and FIG. 1).

In re claims 16, 18 and 19, **AAPA** discloses encapsulating the semiconductor wafer substrate assembly subsequent to selection of operational mode; forming a V_{SS} power buss and a V_{SSQ} power buss during formation of the first and second internal power buses; and electrically connecting the first conductive pad with the second conductive pad to electrically connect the V_{SS} power bus with the V_{SSQ} power bus (pages 2-4, paragraphs [0004]-[0010]).

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6-19, and 24-32 have been considered but are moot in view of the new ground(s) of rejection.

In response to Applicant's argument that **Saito** does not teach or suggest the selective connection of first and second pads or second or third pads to enable a wafer section to function with a first or second operation mode, examiner respectfully disagree, Applicants are directed to the new ground(s) of rejection presented in this Office Action where the newly discovered references **Tavana et al.** (U.S. Patent 6,094,065) in view of **(JP 6-232537)** disclose a method used to form a semiconductor device comprising: forming a semiconductor wafer section comprising first, second, and third pads thereon which are electrically separate from each other (**FIGS. 1-8** and related text); forming a first circuit portion **(FIG. 8: 12)**; forming a second circuit portion **(FIG. 8: 36)** and electrically isolated from the first circuit portion; forming a third circuit portion **(FIG. 8: 14)** and electrically isolated from the first and second circuit portions; and selectively electrically connecting together either the first and second circuit portions or the second and third circuit portions, wherein the semiconductor wafer section is enabled to function with a first operation mode if the first and second pads are electrically connected together, and is enabled to function with a second operational mode different from the first operational mode if the second and third pads are electrically connected together (col. 7, lines 8-15 and **FIGS. 2-8**).

Tavana does not explicitly disclose wherein the first circuit portion electrically coupled with a first pad, the second circuit portion electrically coupled with the second pad, and the third circuit portion electrically coupled with the third pad and selectively electrically connecting together either the first and second pads or the second and third pads to electrically connect either the first and second circuit portions or the second and third circuit portions. **(JP 6-232537)** discloses forming a first circuit portion (**FIGS. 3a-c: 11** (located on the left side in the drawing)) electrically coupled with a first pad (**FIGS. 3a-c: 12** (located on the left side in the drawing), a second circuit portion (FIGS. 3a-c: 11 (located on the right side in the drawing)) electrically coupled with the second pad (**FIGS. 3a-c: 12** (located on the right side in the drawing)) and electrically connecting together the first and second pads to electrically connect the first and second circuit portions **(FIGS. 3b-c: 13)** (JP 6-232537 translation, pages 1-2).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
January 13, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER